Intel® Desktop Board D865PCK

Technical Product Specification

February 2005

Order Number: C99878-001

The Intel® Desktop Board D865PCK may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D865PCK Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D865PCK Technical Product Specification.	February 2005

This product specification applies to only standard Intel® Desktop Board D865PCK with BIOS identifier CK86510J.86A.

Changes to this specification will be published in the Intel Desktop Board D865PCK Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board D865PCK. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the Desktop Board D865PCK and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the Desktop Board D865PCK
2	A map of the resources of the Desktop Board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

INTEGRATOR'S NOTES

Integrator's notes are used to call attention to information that may be useful to system integrators.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the Desktop Board D865PCK, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

Figures

Tables

1 Product Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of the Desktop Board D865PCK.

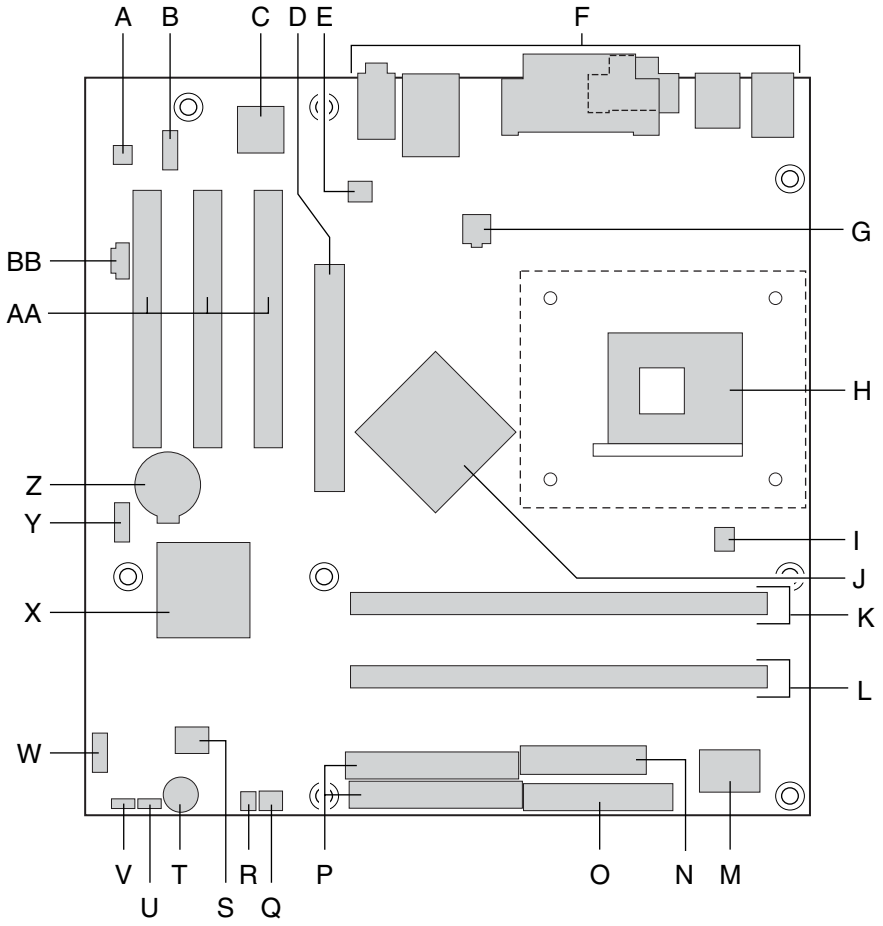
Table 1. Feature Summary

Form Factor	microATX (9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters])
Processor	• Support for an Intel® Pentium® 4 processor in an mPGA478 socket with a 400 or 533 MHz system bus • Support for an Intel® Celeron® processor in an mPGA478 socket with a 400 MHz system bus
Memory	• Two 184-pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets • Support for DDR 333 and DDR 266 DIMMs • Support for up to 2 GB of system memory
Chipset	Intel® 865P Chipset, consisting of: • Intel® 82865P Memory Controller Hub (MCH) • Intel® 82801EB I/O Controller Hub (ICH5) • 8 Mbit Firmware Hub (FWH)
Video	Universal 0.8 V / 1.5 V AGP 3.0 connector (with integrated retention mechanism) supporting 1x, 4x, and 8x AGP cards or an AGP Digital Display (ADD) card
Audio	Audio subsystem using the Realtek ALC202 codec
I/O Control	LPC Bus I/O controller
USB	Support for USB 2.0 devices
Peripheral Interfaces	• Six USB ports • One serial port • One parallel port • Two Parallel ATA IDE interfaces with UDMA 33, ATA-66/100 support • One diskette drive interface • PS/2* keyboard and mouse ports
LAN Support	10/100 Mbits/sec LAN subsystem using the Intel® 82562EZ Platform LAN Connect (PLC) device
BIOS	• BIOS resident in the 8 Mbit FWH • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Suspend to RAM support • Wake on PCI, RS-232, front panel, PS/2 devices, and USB ports
Expansion Capabilities	Three PCI bus add-in card connectors (SMBus routed to PCI bus connector 2)

For information about	Refer to
Available configurations for the Desktop Boards D865PCK	Section 1.2, page 13

1.1.2 Board Layout

Figure 1 shows the location of the major components.



A	Audio codec	O	Diskette drive connector
B	Front panel audio connector	P	Parallel ATE IDE connectors
C	Ethernet PLC device (optional)	Q	Front chassis fan connector
D	AGP connector	R	Chassis intrusion connector
E	Rear chassis fan connector	S	8 Mbit Firmware Hub (FWH)
F	Back panel connectors	T	Speaker
G	+12V power connector (ATX12V)	U	BIOS Setup configuration jumper block
H	mPGA478 processor socket	V	Auxiliary front panel power LED connector
I	Processor fan connector	W	Front panel connector
J	Intel 82865P MCH	X	Intel 82801EB I/O Controller Hub (ICH5)
K	DIMM Channel A socket	Y	Front panel USB connector
L	DIMM Channel B socket	Z	Battery
M	I/O controller	AA	PCI bus add-in card connectors
N	Power connector	BB	ATAPI CD-ROM connector

Figure 1. Desktop Board D865PCK Components

1.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.

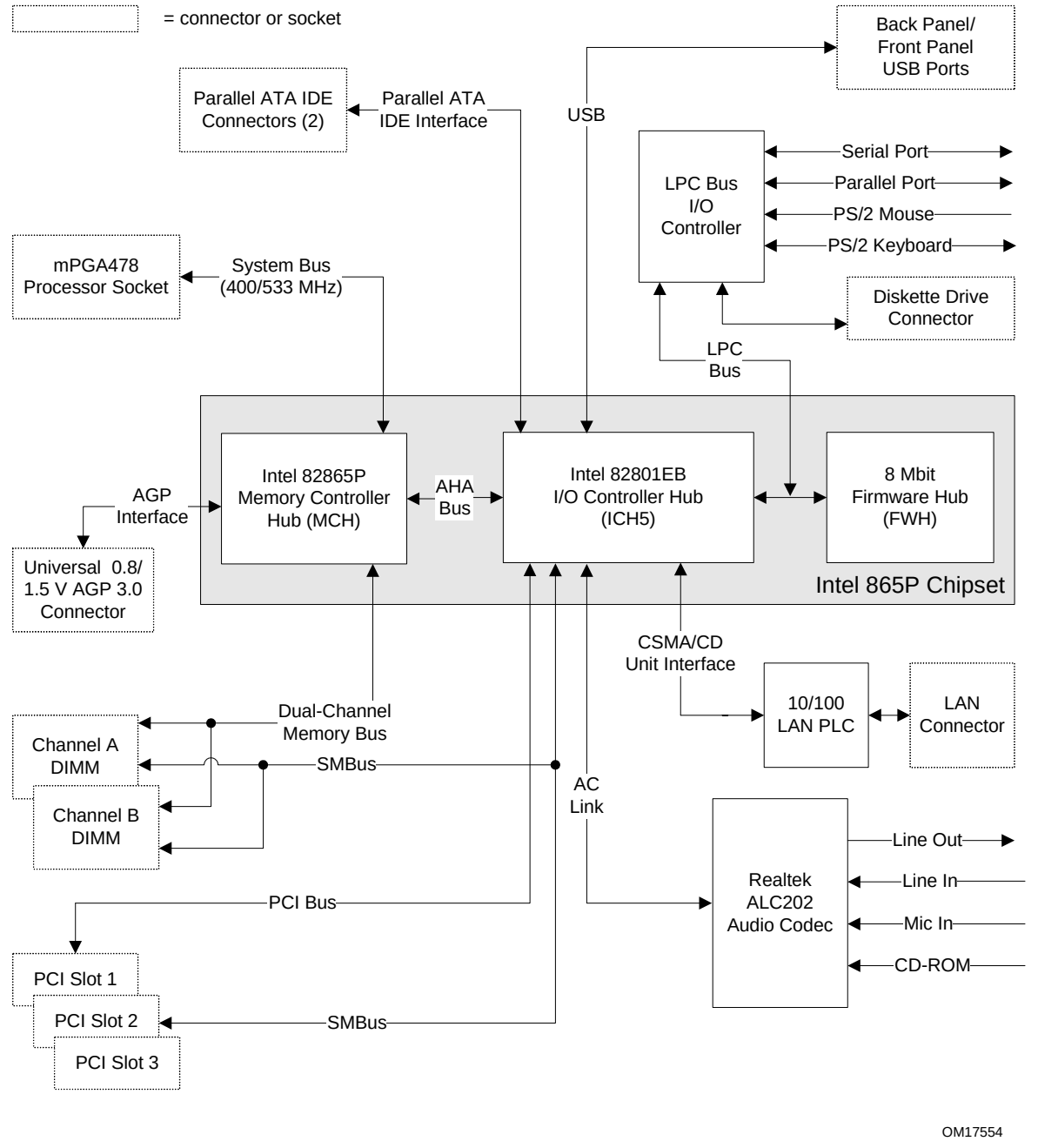


Figure 2. Block Diagram

1.2 Online Support

To find information about…	Visit this World Wide Web site:
Intel® Desktop Board D865PCK under "Desktop Board Products" or "Desktop Board Support"	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Available configurations for the Desktop Board D865PCK	http://developer.intel.com/design/motherbd/ck/ck_available.htm
Processor data sheets	http://www.intel.com/design/litcentr
ICH5 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.3 Processor

NOTE

Refer to Thermal Considerations (Section 2.12, page 55) for important information when using an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board.

The board is designed to support the following:

- Intel Pentium 4 processors in an mPGA478 processor socket with a 400 or 533 MHz system bus
- Intel Celeron processors in an mPGA478 processor socket with a 400 MHz system bus

See the Intel web site listed below for the most up-to-date list of supported processors.

For information about…	Refer to:
Supported processors for the D865PCK board	http://www.intel.com/design/motherbd/ck/ck_proc.htm

CAUTION

Use only the processors listed on web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

INTEGRATOR'S NOTES

- *Use only ATX12V-, SFX12V-, or TFX12V-compliant power supplies. ATX12V, SFX12V, and TFX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V, SFX12V, and TFX12V power supplies to the corresponding connectors on the desktop board, otherwise the board will not boot.*
- *Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.*
- *Refer to Table 2 on page 14 for a list of supported system bus frequency and memory speed combinations.*

For information about	Refer to
Power supply connectors	Section 2.8.2.2, page 40

1.4 System Memory

The board has two DIMM sockets and supports the following memory features:

- 2.5 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:
  - Double-sided DIMMS with x16 organization are not supported.
- 2 GB maximum total system memory
- Minimum total system memory: 64 MB
- Non-ECC DIMMs
- Serial Presence Detect
- DDR333 and DDR266 SDRAM DIMMs

Table 2 lists the supported system bus frequency and memory speed combinations.

Table 2. Supported System Bus Frequency and Memory Speed Combinations

To use this type of DIMM…	The processor's system bus frequency must be…
DDR333	533 MHz
DDR266	533 or 400 MHz

NOTES

- *Remove the AGP video card before installing or upgrading memory to avoid interference with the memory retention mechanism.*
- *To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.*

Table 3 lists the supported DIMM configurations.

Table 3. Supported Memory Configurations

DIMM Capacity	Configuration	DDR SDRAM Density	DDR SDRAM Organization Front-side/Back-side	Number of DDR SDRAM Devices
64 MB	SS	64 Mbit	8 M x 8/empty	8
64 MB	SS	128 Mbit	8 M x 16/empty	4
128 MB	DS	64 Mbit	8 M x 8/8 M x 8	16
128 MB	SS	128 Mbit	16 M x 8/empty	8
128 MB	SS	256 Mbit	16 M x 16/empty	4
256 MB	DS	128 Mbit	16 M x 8/16 M x 8	16
256 MB	SS	256 Mbit	32 M x 8/empty	8
256 MB	SS	512 Mbit	32 M x 16/empty	4
512 MB	DS	256 Mbit	32 M x 8/32 M x 8	16
512 MB	SS	512 Mbit	64 M x 8/empty	8
1024 MB	DS	512 Mbit	64 M x 8/64 M x 8	16

Note: In the second column, “DS” refers to double-sided memory modules (containing two rows of DDR SDRAM) and “SS” refers to single-sided memory modules (containing one row of DDR SDRAM).

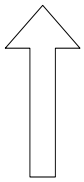
1.4.1 Memory Configurations

The Intel 82865P MCH component provides two features for enhancing memory throughput:

- Dual Channel memory interface. The board has two memory channels, each with a single DIMM socket, as shown in Figure 3
- Dynamic Addressing Mode. Dynamic mode minimizes overhead by reducing memory accesses

Table 4 summarizes the characteristics of Dual and Single Channel configurations with and without the use of Dynamic Mode.

Table 4. Characteristics of Dual/Single Channel Configuration with/without Dynamic Mode

Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	DIMMs matched (Example configuration shown in Figure 4)
	Single Channel with Dynamic Mode	Single DIMM (Example configuration shown in Figure 5)
	Single Channel without Dynamic Mode	DIMMs not matched (Example configuration shown in Figure 6)
Lowest		

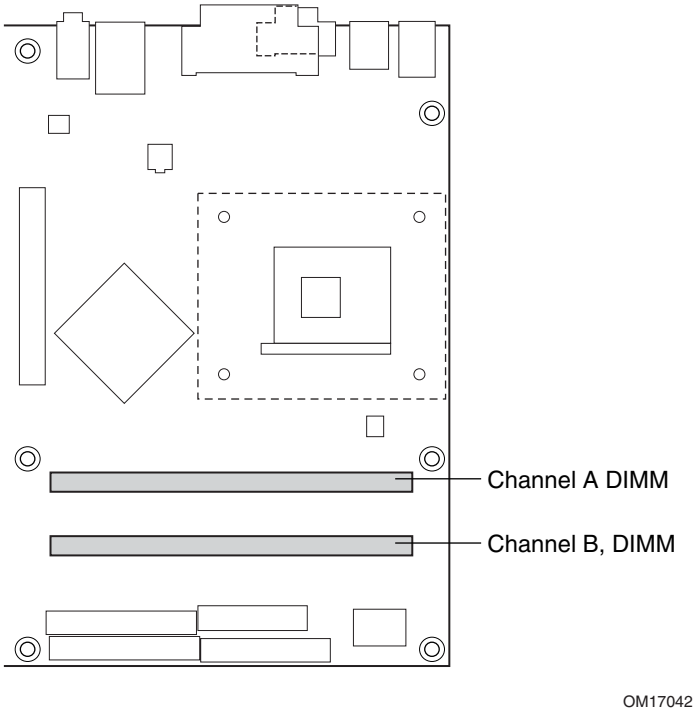
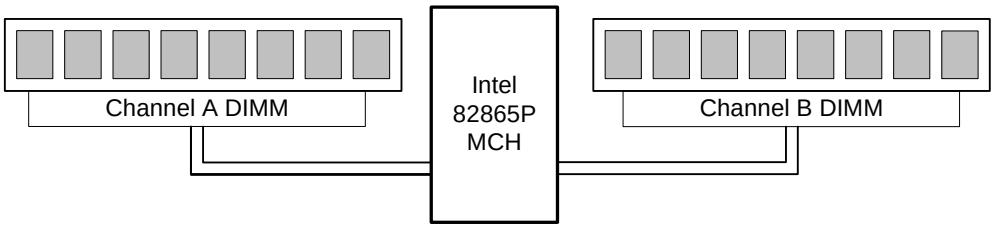


Figure 3. Memory Channel Configuration

Dual Channel Configuration with Dynamic Mode
(DIMMs matched)



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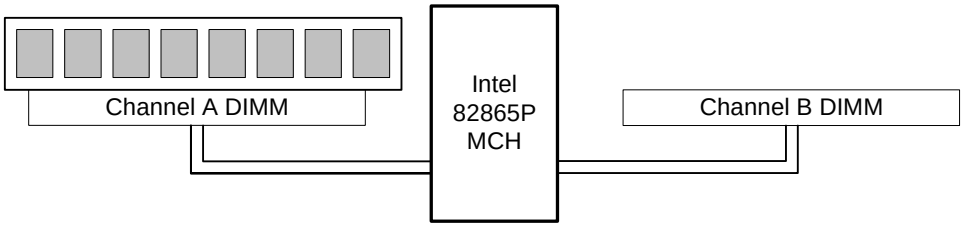
Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	DIMMs matched
↑	Single Channel with Dynamic Mode	Single DIMM
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 4. Example of Dual Channel Configuration with Dynamic Mode

Single Channel Configuration with Dynamic Mode
(Single DIMM)



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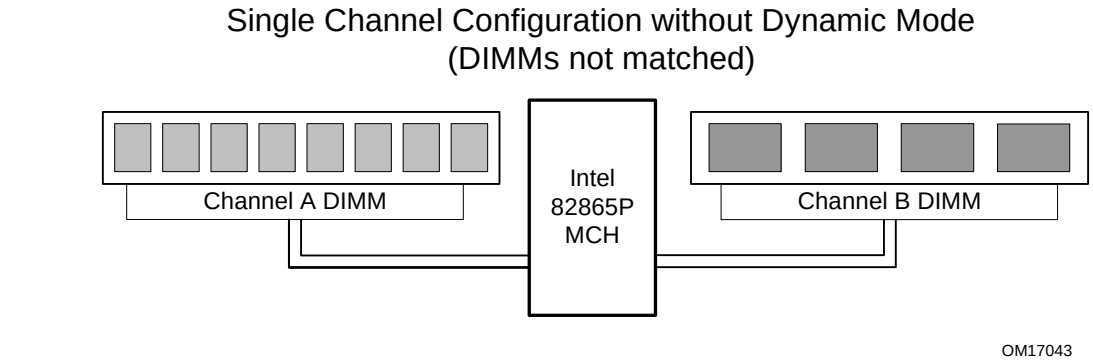
Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	DIMMs matched
↑	Single Channel with Dynamic Mode	Single DIMM
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 5. Example of Single Channel Configuration with Dynamic Mode



Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	DIMMs matched
⇧	Single Channel with Dynamic Mode	Single DIMM
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 6. Example of Single Channel Configuration without Dynamic Mode

1.5 Intel® 865P Chipset

The Intel 865P chipset consists of the following devices:

- Intel 82865P Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- Intel 82801EB I/O Controller Hub (ICH5) with AHA bus
- Firmware Hub (FWH)

The MCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH5 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS.

For information about	Refer to
The Intel 865P chipset	http://developer.intel.com/
Resources used by the chipset	Chapter 2

1.5.1 Universal 0.8 V / 1.5 V AGP 3.0 Connector

The AGP connector supports the following:

- 4x, 8x AGP 3.0 add-in cards with 0.8 V I/O
- 1x, 4x AGP 2.0 add-in cards with 1.5 V I/O
- AGP Digital Display (ADD) cards

AGP is a high-performance interface for graphics-intensive applications, such as 3D applications. While based on the *PCI Local Bus Specification*, Rev. 2.2, AGP is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent efficiency

INTEGRATOR'S NOTES

- *AGP 2x operation is not supported.*
- *Install memory in the DIMM sockets prior to installing the AGP video card to avoid interference with the memory retention mechanism.*
- *The AGP connector is keyed for Universal 0.8 V AGP 3.0 cards or 1.5 V AGP 2.0 cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.*

For information about	Refer to
The location of the AGP connector	Figure 1, page 11

1.5.2 USB

The board supports up to six USB 2.0 ports, supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers.

The ICH5 provides the USB controller for all ports. The port arrangement is as follows:

- Two ports are implemented with stacked back panel connectors, adjacent to the PS/2 connectors
- Two ports are implemented with stacked back panel connectors, adjacent to the audio connectors
- Two ports are routed to a front panel USB connector

NOTES

- *Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.*
- *Native USB 2.0 support has been tested with drivers for Windows* 2000 (with Service Pack 3) and Windows XP (with Service Pack 1) and is not currently supported by any other operating system. Check Intel's Desktop Board website for possible driver updates for other operating systems.*

For information about	Refer to
The location of the USB connectors on the back panel	Figure 8, page 38
The location of the front panel USB connector	Figure 12, page 46

1.5.3 IDE Support

The board provides two Parallel ATA IDE connectors, which support a total of four devices (two per connector). The ICH5's Parallel ATA IDE controller has two independent bus-mastering Parallel ATA IDE interfaces that can be independently enabled. The Parallel ATA IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH5's ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The Parallel ATA IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

For information about	Refer to
The location of the Parallel ATA IDE connectors	Figure 11, page 45

1.5.4 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

1.6 I/O Controller

The I/O controller provides the following features:

- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems

- PS/2-style mouse and keyboard interfaces
- Interface for one 1.44 MB or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M172 I/O controller	http://www.smsc.com
National Semiconductor PC87372 I/O Controller	http://www.national.com/

1.6.1 Serial Port

The board has one serial port connector located on the back panel. The serial port supports data transfers at speeds up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port A connector	Figure 8, page 38

1.6.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

For information about	Refer to
The location of the parallel port connector	Figure 8, page 38

1.6.3 Diskette Drive Controller

The I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

For information about	Refer to
The location of the diskette drive connector on the D865PCK board	Figure 11, page 45

1.6.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 8, page 38

1.7 Audio Subsystem

The board provides an audio subsystem based on the Realtek ALC202 codec.

1.7.1 Realtek ALC202-based Audio Subsystem

The Realtek ALC202-based audio subsystem consists of the following devices:

- Intel 82801EB I/O Controller Hub (ICH5)
- Realtek ALC202 audio codec

The audio subsystem includes these features:

- Signal-to-noise ratio ≥ 90 dB
- Supports wake events (driver dependent)
- Mic in pre-amp that supports dynamic, condenser, and electret microphones

The back panel audio connectors for this audio subsystem including the following:

- Line out
- Line in
- Mic in

1.7.2 Audio Connectors

1.7.2.1 Front Panel Audio Connector

A 2 x 5-pin connector provides mic in and line out signals for front panel audio connectors.

For information about	Refer to
The location of the connector	Figure 9, page 40
The signal names of the front panel audio connector	Table 16, page 41

NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 50 for more information.

1.7.2.2 ATAPI CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI CD-ROM connector	Figure 9, page 40
The signal names of the ATAPI CD-ROM connector	Table 15, page 41

1.7.3 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.2, page 13

1.8 LAN Subsystem

The 10/100 Mbits/sec LAN subsystem consists of the following:

- Intel 82562EZ Platform LAN Connect (PLC) device for 10/100 Mbits/sec Ethernet LAN connectivity
- Intel 82801EB ICH5 (with its CSMA/CD interface)
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- PCI bus master interface
- CSMA/CD protocol engine
- PCI power management
  - — Supports ACPI technology
  - — Supports LAN wake capabilities

1.8.1 Intel® 82562EZ Physical Layer Interface Device

The Intel 82562EZ provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- Full device driver compatibility
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.8.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 7 below).

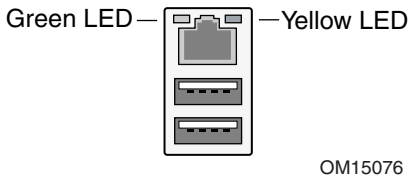


Figure 7. LAN Connector LED Locations

Table 5 describes the LED states when the board is powered up and the 10/100 Mbits/sec LAN subsystem is operating.

Table 5. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	LAN link is not established
	On	LAN link is established
	Blinking	LAN activity is occurring
Yellow	Off	10 Mbits/sec data rate is selected
	On	100 Mbits/sec data rate is selected

1.8.3 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 13

1.9 Chassis Intrusion and Detection

The Desktop Board D865PCK supports a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the closed position.

1.10 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support

1.10.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the Desktop Board D865PCK requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 8 on page 26)
- Support for a front panel power and sleep mode switch

Table 6 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 6. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

1.10.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 7 lists the power states supported by the Desktop Board D865PCK and along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 7. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.10.1.2 Wake-up Devices and Events

Table 8 lists the devices or specific events that can wake the computer from specific states.

Table 8. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
LAN	S1, S3, S4, S5 (Note)
Modem (back panel Serial Port A)	S1, S3
PME# signal	S1, S3, S4, S5 (Note)
Power switch	S1, S3, S4, S5
PS/2 devices	S1, S3
RTC alarm	S1, S3, S4, S5
USB	S1, S3

Note: For LAN and PME# signal, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.10.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The Desktop Board D865PCK provides several power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# signal wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

NOTE

The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

1.10.2.1 Power Connector

ATX12V-, SFX12V-, and TFX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the power connector	Figure 9, page 40
The signal names of the power connector	Table 20, page 43

1.10.2.2 LAN Wake Capabilities

CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the Desktop Board D865PCK support LAN wake capabilities with ACPI in the following ways:

- The PCI bus PME# signal for PCI 2.2 compliant LAN designs
- The onboard LAN subsystem

1.10.2.3 Instantly Available PC Technology

CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the Desktop Board D865PCK to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 8 on page 26 lists the devices and events that can wake the computer from the S3 state.

The Desktop Board D865PCK supports the *PCI Bus Power Management Interface Specification*. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

1.10.2.4 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.10.2.5 Wake from USB

USB bus activity wakes the computer from ACPI S1 or S3 states.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.10.2.6 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

1.10.2.7 PME# Signal Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in BIOS).

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 9 describes the system memory map, Table 10 lists the DMA channels, Table 11 shows the I/O map, Table 12 defines the PCI configuration space map, and Table 13 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 9 lists the system memory map.

Table 9. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 2097152 K	100000 - 7FFFFFFF	2047 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 DMA Channels

Table 10. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.4 Fixed I/O Map

Table 11. I/O Map

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the Desktop Board D865PCK. Refer to the ICH5 data sheet for dynamic addressing information.
0170 - 0177	8 bytes	Secondary Parallel ATA IDE channel command block
01F0 - 01F7	8 bytes	Primary Parallel ATA IDE channel command block
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4
02F8 - 02FF (Note 1)	8 bytes	COM2
0374 - 0377	4 bytes	Secondary Parallel ATA IDE channel control block
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82865P MCH
03C0 - 03DF	32 bytes	Intel 82865P MCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel
03F4 – 03F7	1 byte	Primary Parallel ATA IDE channel control block
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary Parallel ATA IDE bus master registers
FFA8 - FFAF	8 bytes	Secondary Parallel ATA IDE bus master registers

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH5 address aliasing. The ICH5 data sheet provides more information on address aliasing.

For information about	Refer to
Obtaining the ICH5 data sheet	Section 1.2 on page 13

2.5 PCI Configuration Space Map

Table 12. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82865P component
00	01	00	Host to AGP bridge (virtual PCI-to-PCI)
00	03	00	PCI to CSA Bridge (virtual PCI-to-PCI)
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801EB ICH5 PCI to LPC bridge
00	1F	01	Parallel ATA IDE controller
00	1F	03	SMBus controller
00	1F	05	AC '97 audio controller
00	1F	06	AC '97 modem controller
00	1D	00	USB UHCI controller 1
00	1D	01	USB UHCI controller 2
00	1D	02	USB UHCI controller 3
00	1D	03	USB UHCI controller 4
00	1D	07	EHCI controller
01	00	00	AGP add-in card
(Note)	01	00	Intel® 82547EI Gigabit LAN PLC (if present)
(Note)	08	00	Intel 82562EZ 10/100 Mbits/sec LAN PLC (if present)
(Note)	00	00	PCI bus connector 1
(Note)	01	00	PCI bus connector 2
(Note)	02	00	PCI bus connector 3

Note: Bus number = 03 when the Intel 82547EI Gigabit LAN controller is used. Otherwise, bus number = 02.

2.6 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH5 component. The PIC is supported in Windows 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and supports a total of 24 interrupts.

Table 13. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option)/User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for ICH5 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE
15	Secondary IDE
16 (Note 2)	USB UHCI controller 1 / USB UHCI controller 4 (through PIRQA)
17 (Note 2)	AC ‘97 audio/modem/User available (through PIRQB)
18 (Note 2)	ICH5 USB controller 3 (through PIRQC)
19 (Note 2)	ICH5 USB controller 2 (through PIRQD)
20 (Note 2)	ICH5 LAN (through PIRQE)
21 (Note 2)	User available (through PIRQF)
22 (Note 2)	User available (through PIRQG)
23 (Note 2)	ICH5 USB 2.0 EHCI controller/User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH5 has eight Programmable Interrupt Request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the Desktop Boards D865PCK and therefore share the same interrupt. Table 14 shows an example of how the PIRQ signals are routed.

For example, using Table 14 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 3. In PCI bus connector 3, INTA is connected to PIRQB, which is already connected to the ICH5 audio controller. The add-in card in PCI bus connector 3 now shares an interrupt with the onboard interrupt source.

Table 14. PCI Interrupt Routing Map

PCI Interrupt Source	ICH5 PIRQ Signal Name							
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**	**PIRQE**	**PIRQF**	**PIRQG**	**PIRQH**
AGP connector	INTA	INTB						
ICH5 USB UHCI controller 1	INTA							
SMBus controller		INTB						
ICH5 USB UHCI controller 2				INTB				
AC '97 ICH5 Audio		INTB						
ICH5 LAN					INTA			
ICH5 USB UHCI controller 3			INTC					
ICH5 USB UHCI controller 4	INTA							
ICH5 USB 2.0 EHCI controller								INTD
PCI bus connector 1					INTD	INTA	INTB	INTC
PCI bus connector 2					INTC	INTB	INTA	INTD
PCI bus connector 3	INTD	INTA	INTB	INTC				

NOTE

In PIC mode, the ICH5 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 13 for the allocation of PIRQ lines to IRQ signals in APIC mode.

2.8 Connectors

⚠ CAUTION

Only the following connectors have overcurrent protection: back panel USB, front panel USB, and PS/2.

The other internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into these groups:

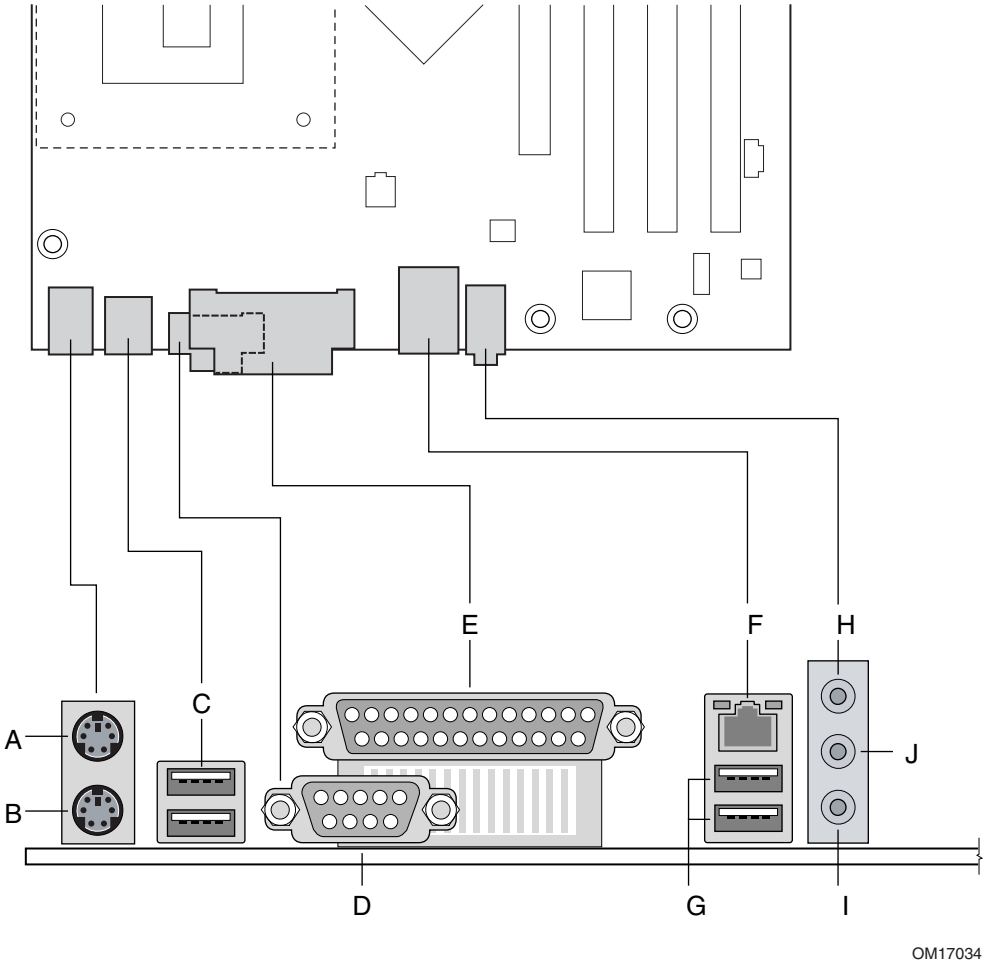
- Back panel I/O connectors (see page 38)
  - PS/2 keyboard and mouse
  - USB (four ports)
  - Parallel port
  - Serial port A
  - LAN
  - Audio (line out, line in, and mic in)
- Internal I/O connectors (see page 39)
  - Audio (ATAPI CD-ROM and front panel audio)
  - Fans [three]
  - Power
  - Add-in boards (PCI and AGP)
  - Parallel ATA IDE
  - Diskette drive
  - Chassis intrusion
- External I/O connectors (see page 46)
  - Front panel USB (two connector for four ports)
  - Auxiliary front panel power/sleep/message-waiting LED
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel power LED)

NOTE

When installing the board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, the Parallel ATA IDE connectors, and the DIMM sockets.

2.8.1 Back Panel Connectors

Figure 8 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color	Item	Description	Color
A	PS/2 mouse port	Green	F	LAN	Black
B	PS/2 keyboard port	Purple	G	USB ports	Black
C	USB ports	Black	H	Audio line in	Light blue
D	Serial port A	Teal	I	Mic in	Pink
E	Parallel port	Burgundy	J	Audio line out	Lime green

Figure 8. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio (see page 40)
  - ATAPI CD-ROM
  - Front panel audio
- Power and hardware control (see page 42)
  - Fans [3]
  - ATX12V power
  - Main power
  - Chassis intrusion
- Add-in boards and peripheral interfaces (see page 45)
  - PCI bus
  - AGP
  - IDE
  - Diskette drive

2.8.2.1 Expansion Slots

The board has the following expansion slots:

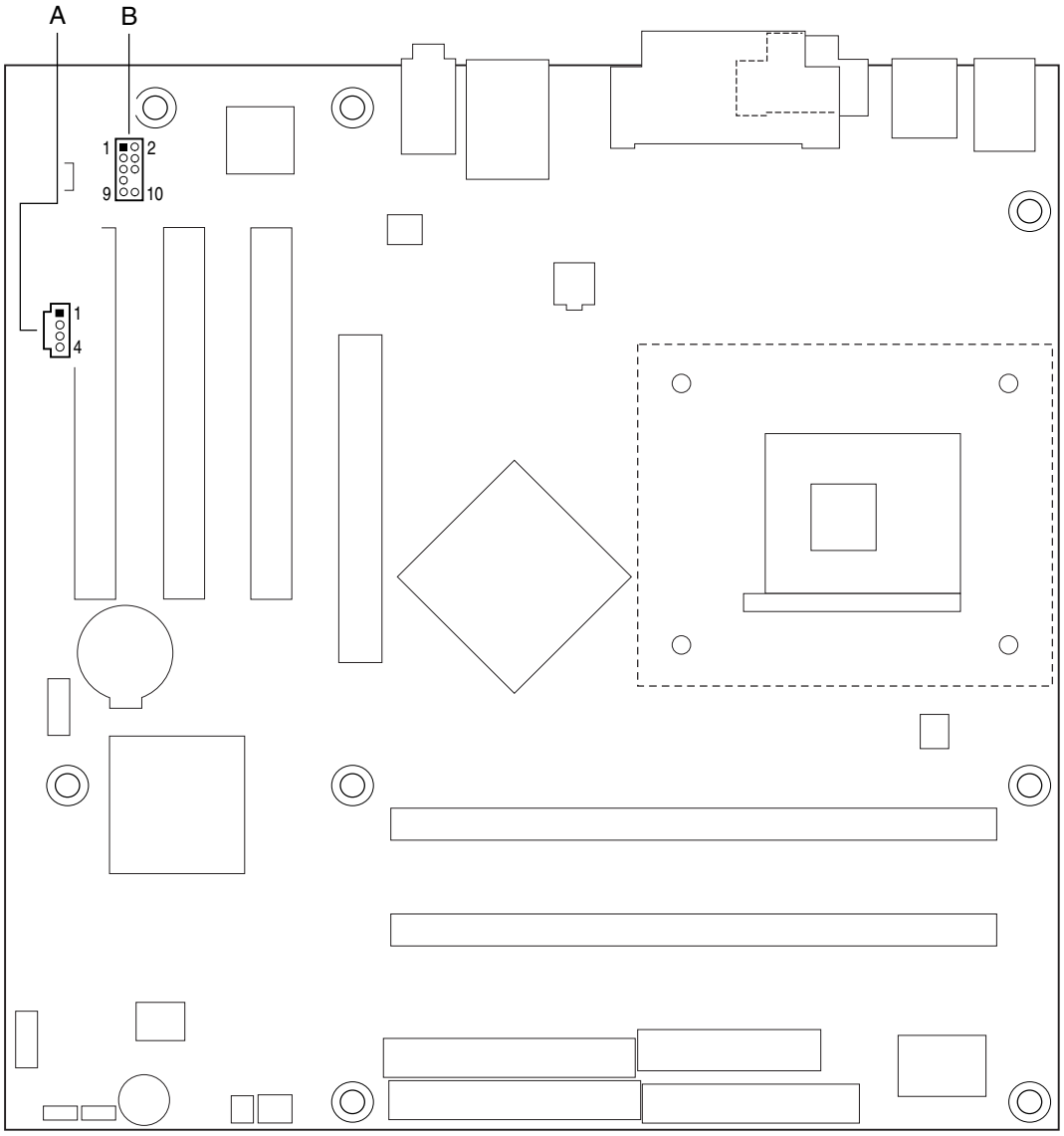
- AGP connector: The AGP connector is keyed for Universal 0.8 V AGP 3.0 cards or 1.5 V AGP 2.0 cards only. Do not install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.
- Three PCI rev 2.2 compliant local bus slots. The SMBus is routed to PCI bus connector 2 only (ATX expansion slot 6). PCI add-in cards with SMBus support can access sensor data and other information residing on the Desktop Board.

NOTE

This document references back-panel slot numbering with respect to processor location on the board. The AGP slot is not numbered. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. Figure 11 (page 45) illustrates the board's PCI slot numbering.

2.8.2.2 Audio Connectors

Figure 9 shows the location of the audio connectors.



Item	Description	For more information see:
A	ATAPI CD-ROM (black)	Table 15
B	Front panel audio	Table 16

Figure 9. Audio Connectors

Table 15. ATAPI CD-ROM Connector

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

Table 16. Front Panel Audio Connector

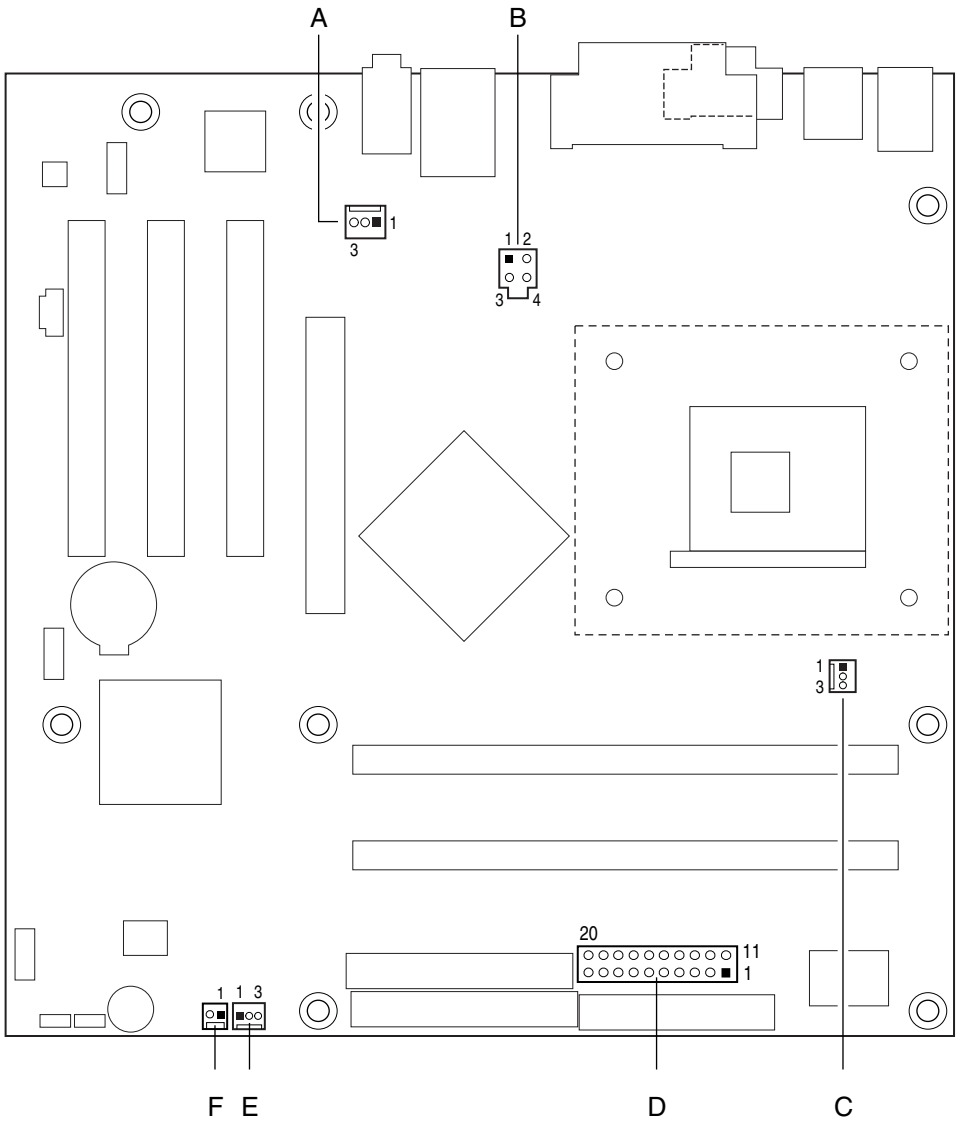
Pin	Signal Name	Pin	Signal Name
1	Mono Mic in	2	Ground
3	Mono Mic Bias	4	+5 V
5	RIGHT_OUT	6	Right channel return
7	No connect	8	Key
9	LEFT_OUT	10	Left channel return

INTEGRATOR'S NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 50 for more information.

2.8.2.3 Power and Hardware Control Connectors

Figure 10 shows the location of the power and hardware control connectors.



Item	Description	For more information see:
A	Rear chassis fan	Table 17
B	+12 V power connector (ATX12V)	Table 18
C	Processor fan	Table 19
D	Main power	Table 20
E	Front chassis fan	Table 21
F	Chassis intrusion	Table 22

Figure 10. Power and Hardware Control Connectors

Table 17. Rear Chassis Fan Connector

Pin	Signal Name
1	Control
2	+12 V
3	REAR_TACH_OUT

INTEGRATOR'S NOTES

- *Use only ATX12V-, SFX12V-, or TFX12V-compliant power supplies with the Desktop Board D865PCK. ATX12V, SFX12V, and TFX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V, SFX12V, and TFX12V power supplies to the corresponding connectors on the desktop board, otherwise the board will not boot.*
- *Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.*

Table 18. ATX12V Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	+12 V	4	+12 V

Table 19. Processor Fan Connector

Pin	Signal Name
1	Control
2	+12 V
3	CPU_FAN_TACH

Table 20. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	No connect
9	+5 V (Standby)	19	+5 V
10	+12 V	20	+5 V

Table 21. Front Chassis Fan Connector

Pin	Signal Name
1	Control
2	+12 V
3	Tach

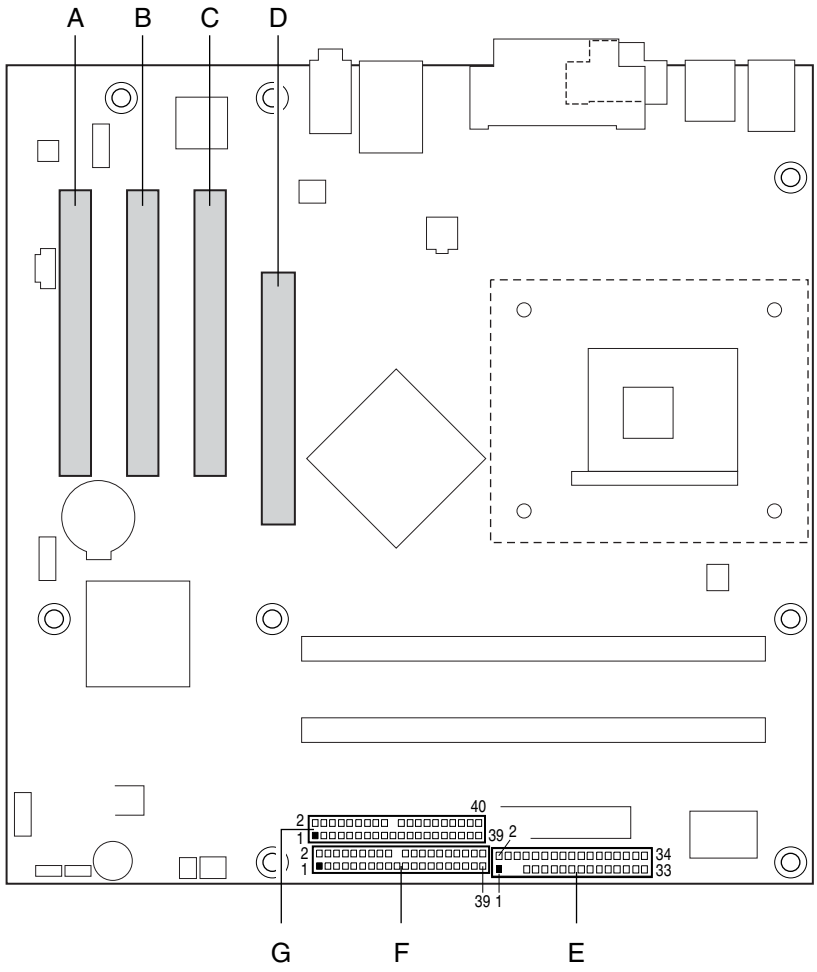
Table 22. Chassis Intrusion Connector

Pin	Signal Name
1	Intruder
2	Ground

2.8.2.4 Add-in Board and Peripheral Interface Connectors

Figure 11 shows the location of the add-in board connector and peripheral connectors. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- SMBus signals are routed to PCI bus connector 2. This enables PCI bus add-in boards with SMBus support to access sensor data on the Desktop Board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.



Item	Description	Item	Description
A	PCI bus connector 3	E	Diskette drive
B	PCI bus connector 2	F	Primary IDE [black]
C	PCI bus connector 1	G	Secondary IDE [white]
D	AGP connector		

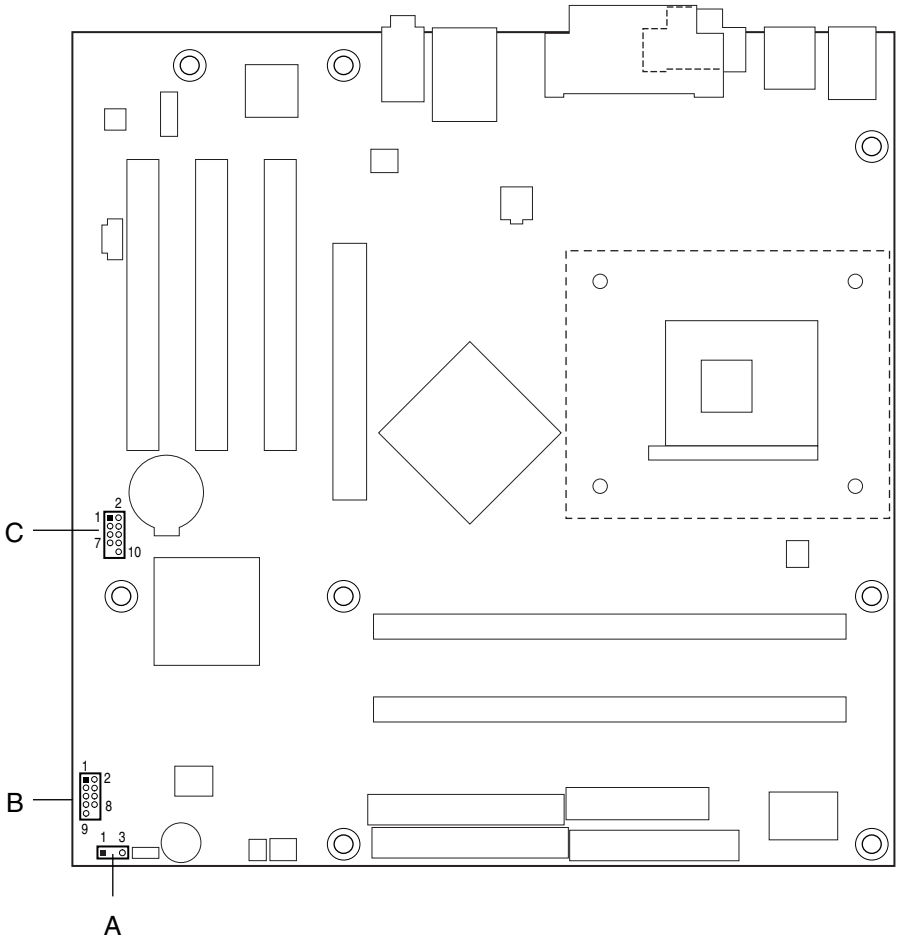
Figure 11. D865PCK Add-in Board and Peripheral Interface Connectors

INTEGRATOR'S NOTES

- *The AGP connector is keyed for Universal 0.8 V AGP 3.0 cards or 1.5 V AGP 2.0 cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.*
- *Not all PCI video cards can be used in PCI bus connectors 1 and 2 (the PCI bus connectors closest to the processor). To avoid clearance problems, install PCI video cards in PCI bus connector 3.*

2.8.3 External I/O Connectors

Figure 12 shows the locations of the external I/O connectors.



Item	Description	Color	For more information see:
A	Auxiliary front panel power/sleep/message-waiting LED	Black	Table 23
B	Front panel	White	Table 24
C	Front panel USB	Black	Figure 14

Figure 12. External I/O Connectors

2.8.3.1 Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pins 1 and 3 of this connector duplicate the signals on pins 2 and 4 of the front panel connector.

Table 23. Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.8.3.2 Front Panel Connector

This section describes the functions of the front panel connector. Table 24 lists the signal names of the front panel connector. Figure 13 is a connection diagram for the front panel connector.

Table 24. Front Panel Connector

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
Hard Drive Activity LED				**Power LED**			
1	HD_PWR	Out	Hard disk LED pull-up (750 Ω) to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
Reset Switch				**On/Off Switch**			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Power				**Not Connected**			
9	+5 V		Power	10	N/C		Not connected

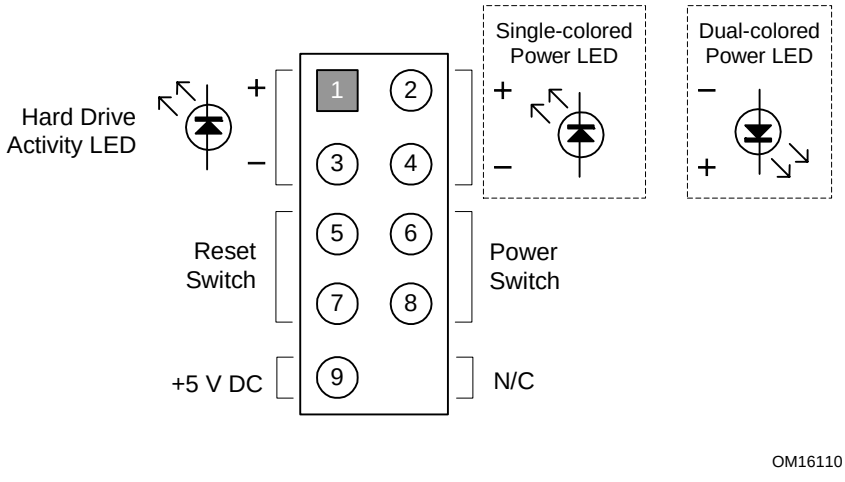


Figure 13. Connection Diagram for Front Panel Connector

2.8.3.2.1 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires an IDE hard drive connected to an onboard IDE connector.

2.8.3.2.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.8.3.2.3 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a one- or two-color LED. Table 25 shows the possible states for a one-color LED. Table 26 shows the possible states for a two-color LED.

Table 25. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 26. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.2.4 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.3.3 Front Panel USB Connectors

Figure 14 is a connection diagram for the front panel USB connector.

INTEGRATOR'S NOTES

- *The +5 V DC power on the USB connector is fused.*
- *Pins 1, 3, 5, and 7 comprise one USB port.*
- *Pins 2, 4, 6, and 8 comprise one USB port.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

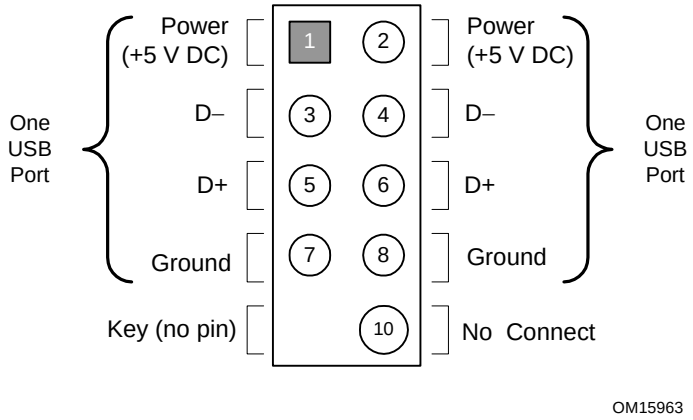


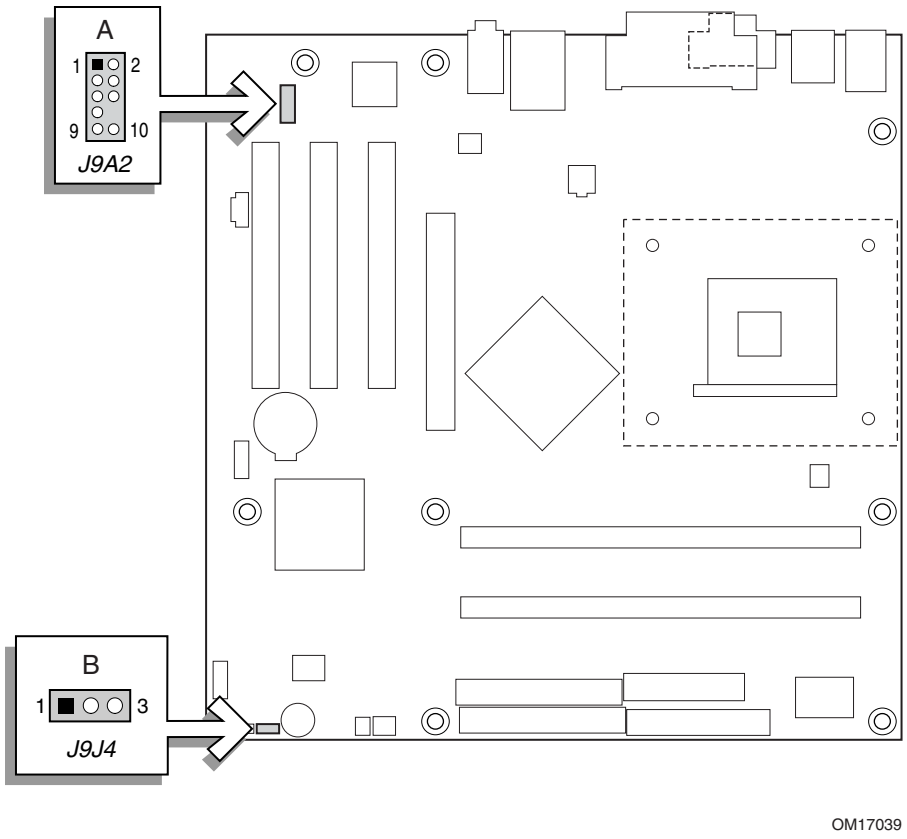
Figure 14. Connection Diagram for Front Panel USB Connector

2.9 Jumper Blocks

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 15 shows the location of the jumper blocks.



Item	Description	Reference Designator
A	Front panel audio connector/jumper block	J9A2
B	BIOS Setup configuration jumper block	J9J4

Figure 15. Location of the Jumper Blocks

2.9.1 Front Panel Audio Connector/Jumper Block

This connector has two functions:

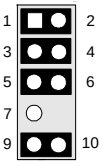
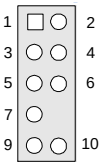
- With jumpers installed, the audio line out signals are routed to the back panel audio line out connector.
- With jumpers removed, the connector provides audio line out and mic in signals for front panel audio connectors.

Table 27 describes the two configurations of this connector/jumper block.

CAUTION

Do not place jumpers on this block in any configuration other than the one described in Table 27. Other jumper configurations are not supported and could damage the Desktop Board.

Table 27. Front Panel Audio Connector/Jumper Block

Jumper Setting		Configuration
	1 and 2 3 and 4 5 and 6 9 and 10	Audio line out signals are routed to the back panel audio line out connector. The back panel audio line out connector is shown in Figure 8 on page 38.
	No jumpers installed	Audio line out and mic in signals are available for front panel audio connectors. Table 16 on page 41 lists the names of the signals available on this connector when no jumpers are installed.

INTEGRATOR'S NOTE

When the jumpers are removed and this connector is used for front panel audio, the back panel audio line out and mic in connectors are disabled.

2.9.2 BIOS Setup Configuration Jumper Block

The 3-pin jumper block determines the BIOS Setup program's mode. Table 28 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

Table 28. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

2.10 Mechanical Considerations

2.10.1 Form Factor

The Desktop Board D865PCK is designed to fit into either a microATX or an ATX-form-factor chassis. Figure 16 illustrates the mechanical form factor for the Desktop Board D865PCK. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

NOTE

When installing the Desktop Board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, and the IDE connector, and the DIMM sockets.

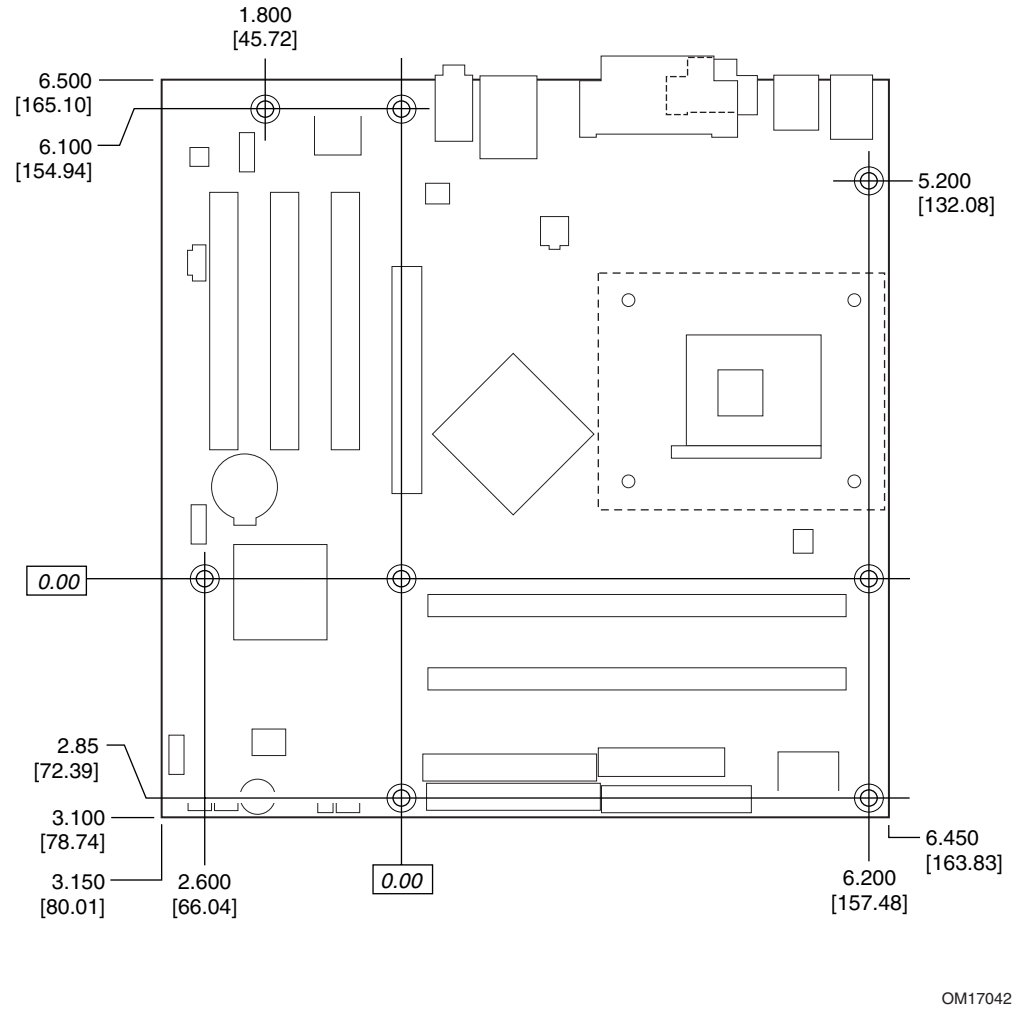


Figure 16. Desktop Board D865PCK Dimensions

2.10.2 I/O Shield

The back panel I/O shield for the Desktop Board D865PCK must meet specific dimension and material requirements. Systems based on this Desktop Board need the back panel I/O shield to pass certification testing. Figure 17 shows the I/O shield. Dimensions are given in inches to a tolerance of ±0.02 inches.

The figure also indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification.

NOTE

The I/O shield drawings in this document are for reference only. An I/O shield compliant with the ATX chassis specification 2.03 is available from Intel.

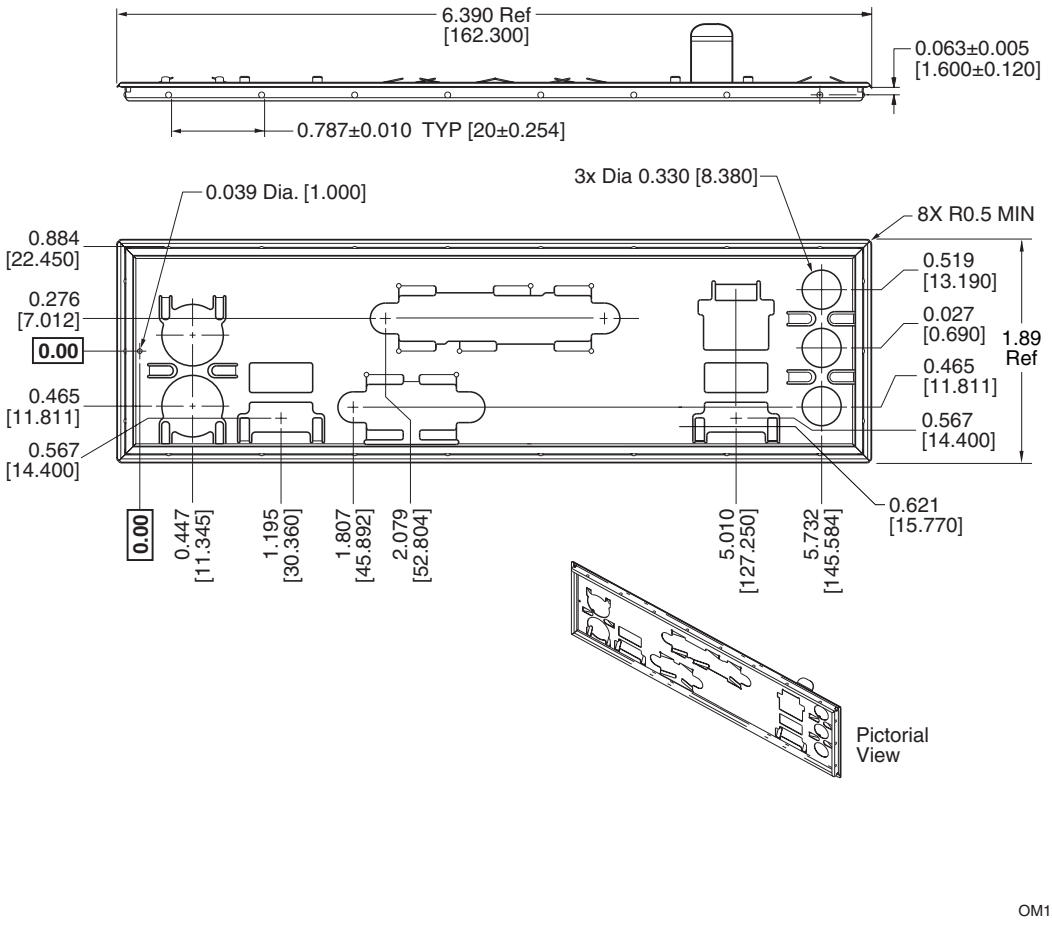


Figure 17. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 DC Loading

Table 29 lists the DC loading characteristics of the board. This data is based on a DC analysis of all active components within the board that impact its power delivery subsystems. The analysis does not include PCI add-in cards. Minimum values assume a light load placed on the board that is similar to an environment with no applications running and no USB current draw. Maximum values assume a load placed on the board that is similar to a heavy gaming environment with a 500 mA current draw per USB port. These calculations are not based on specific processor values or memory configurations but are based on the minimum and maximum current draw possible from the board's power delivery subsystems to the processor, memory, and USB ports.

Use the datasheets for add-in cards, such as PCI, to determine the overall system power requirements. The selection of a power supply at the system level is dependent on the system's usage model and not necessarily tied to a particular processor speed.

Table 29. DC Loading Characteristics

		DC Current at:				
Mode	**DC Power**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Minimum loading	190.00 W	5.00 A	11.00 A	9.00 A	0.03 A	0.60 A
Maximum loading	286.00 W	11.00 A	15.00 A	13.00 A	0.10 A	1.38 A

2.11.2 Add-in Board Considerations

The boards are designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards for a fully loaded Desktop Board D865PCK (all three expansion slots and the AGP slot filled) must not exceed 8 A.

2.11.3 Fan Connector Current Capability

⚠ CAUTION

The processor fan must be connected to the processor fan connector, not to a chassis fan connector. Connecting the processor fan to a chassis fan connector may result in onboard component damage that will halt fan operation.

Table 30 lists the current capability of the fan connectors.

Table 30. Fan Connector Current Capability

Fan Connector	Maximum Available Current
Processor fan	1600 mA
Front chassis fan	600 mA
Rear chassis fan	600 mA

2.11.4 Power Supply Considerations

CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

System integrators should refer to the power usage values listed in Table 29 when selecting a power supply for use with the board.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

2.12 Thermal Considerations

CAUTION

The use of an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board requires the following:

- *A chassis with appropriate airflow to ensure proper cooling of the components on the board*
- *A processor fan heatsink that meets the thermal performance targets for Pentium 4 processors operating above 2.80 GHz*

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the desktop board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:

http://developer.intel.com/design/motherbd/cooling.htm

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

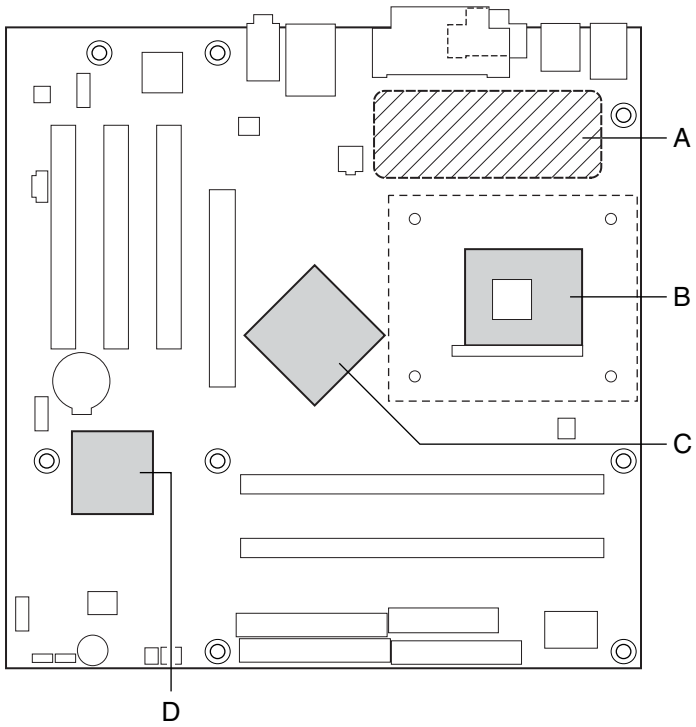
CAUTION

Ensure that the ambient temperature does not exceed the Desktop Board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (item A in Figure 18) can reach a temperature of up to 85 °C in an open chassis.

Figure 18 shows the locations of the localized high temperature zones.



Item	Description
A	Processor voltage regulator area
B	Processor
C	Intel 82865P MCH
D	Intel 82801EB ICH5

Figure 18. Localized High Temperature Zones

Table 31 provides maximum case temperatures for the Desktop Board D865PCK components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the Desktop Board D865PCK.

Table 31. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium 4 processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82865P MCH	99 °C (under bias)
Intel 82801EB ICH5	115 °C (under bias)

For information about	Refer to
Intel Pentium 4 processor datasheets and specification updates	Section 1.2, page 13

2.13 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC. The Desktop Board D865PCK MTBF is 101,425 hours.

2.14 Environmental

Table 32 lists the environmental specifications for the Desktop Board D865PCK.

Table 32. Desktop Board D865PCK Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the Desktop Board's compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 33 lists the safety regulations the Desktop Board D865PCK complies with when correctly installed in a compatible host system.

Table 33. Safety Regulations

Regulation	Title
UL 60950-1:2003/ CSA C22.2 No. 60950-1-03	Information Technology Equipment - Safety - Part 1: General Requirements (USA and Canada)
EN 60950-1:2002	Information Technology Equipment - Safety - Part 1: General Requirements (European Union)
IEC 60950-1:2001, First Edition	Information Technology Equipment - Safety - Part 1: General Requirements (International)

2.15.2 EMC Regulations

Table 34 lists the EMC regulations the Desktop Board D865PCK complies with when correctly installed in a compatible host system.

Table 34. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1998 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 3rd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)
VCCI (Class B)	Voluntary Control for Interference by Information Technology Equipment (Japan)

2.15.2.1 FCC Compliance Statement (USA)

Product Type: D865PCK Desktop Board

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to a different electrical branch circuit from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications to the equipment not expressly approved by Intel Corporation could void the user's authority to operate the equipment.

2.15.2.2 Canadian Compliance Statement

This Class B digital apparatus complies with Canadian ICES-003.

Cet appereil numérique de la classe B est conforme à la norme NMB-003 du Canada.

2.15.3 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product: Intel® Desktop Board D865PCK is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 89/336/EEC (EMC Directive) and Council Directive 73/23/EEC (Safety/Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

CE

This product follows the provisions of the European Directives 89/336/EEC and 73/23/EEC.

Dansk Dette produkt er i overensstemmelse med det europæiske direktiv 89/336/EEC & 73/23/EEC.

Dutch Dit product is in navolging van de bepalingen van Europees Directief 89/336/EEC & 73/23/EEC.

Suomi Tämä tuote noudattaa EU-direktiivin 89/336/EEC & 73/23/EEC määräyksiä.

Français Ce produit est conforme aux exigences de la Directive Européenne 89/336/EEC & 73/23/EEC.

Deutsch Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 89/336/EEC & 73/23/EEC.

Icelandic Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 89/336/ EEC & 73/23/EEC.

Italiano Questo prodotto è conforme alla Direttiva Europea 89/336/EEC & 73/23/EEC.

Norsk Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 89/336/ EEC & 73/23/EEC.

Portuguese Este produto cumpre com as normas da Diretiva Européia 89/336/EEC & 73/23/EEC.

Español Este producto cumple con las normas del Directivo Europeo 89/336/EEC & 73/23/EEC.

Svenska Denna produkt har tillverkats i enlighet med EG-direktiv 89/336/EEC & 73/23/EEC.

2.15.4 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

2.15.4.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

2.15.4.2 Recycling Considerations

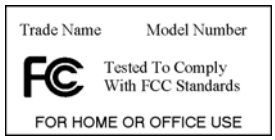
Intel encourages its customers to recycle its products and their components (e.g., batteries, circuit boards, plastic enclosures, etc.) whenever possible. In the U.S., a list of recyclers in your area can be found at:
http://www.eiae.org/

In the absence of a viable recycling option, products and their components must be disposed of in accordance with all applicable local environmental regulations.

2.15.5 Product Certification Markings (Board Level)

Table 35 lists the board's product certification markings.

Table 35. Product Certification Markings

Description	Marking
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Desktop Boards: E210882 (component side).	
FCC Declaration of Conformity logo mark for Class B equipment; includes Intel name and D865PCK model designation (component side).	
CE mark. Declares compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.	
Australian Communications Authority (ACA) C-Tick mark. Includes adjacent Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.	
Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	V-0 or 94V-0

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The BIOS is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as CK86510J.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

NOTE

The maintenance menu is displayed only when the board is in configure mode. Section 2.9.2 on page 51 shows how to put the board in configure mode.

Table 36 lists the BIOS Setup program menu features.

Table 36. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features and power supply controls	Selects boot options	Saves or discards changes to Setup program options

Table 37 lists the function keys available for menu screens.

Table 37. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

3.2 BIOS Flash Memory Organization

The Firmware Hub (FWH) includes an 8 Mbit (1024 KB) symmetrical flash memory device.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS automatically configures PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the PCI IDE connector with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and

to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

3.5 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.

5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette or a CD-ROM.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 13

3.6.1 Language Support

The BIOS Setup program and help messages are supported in US English. Additional languages are available in the Integrator's Toolkit utility. Check the Intel website for details.

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 13

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.7.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

3.7.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

3.7.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.7.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program’s Boot Device Priority Submenu). Table 38 lists the boot device menu options.

Table 38. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.8 Fast Booting Systems with Intel® Rapid BIOS Boot

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS

3.8.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.8.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enable Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 39 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 39. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

4 Error Messages and Beep Codes

What This Chapter Contains

4.1 Speaker

The board-mounted speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, page 11

4.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 40).

Table 40. Beep Codes

Type	Pattern	Frequency
Memory error	Three long beeps	1280 Hz
Thermal warning	Four alternating beeps: High tone, low tone, high tone, low tone	High tone: 2000 Hz Low tone: 1600 Hz

4.3 BIOS Error Messages

Table 41 lists the error messages and provides a brief description of each.

Table 41. BIOS Error Messages

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.

4.4 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in PCI bus connector 1.

The following tables provide information about the POST codes generated by the BIOS:

- Table 42 lists the Port 80h POST code ranges
- Table 43 lists the Port 80h POST codes themselves
- Table 44 lists the Port 80h POST sequence

NOTE

In the tables listed above, all POST codes and range values are listed in hexadecimal.

Table 42. Port 80h POST Code Ranges

Range	Category/Subsystem
00 – 0F	Debug codes: Can be used by any PEIM/driver for debug.
10 – 1F	Host Processors: 1F is an unrecoverable CPU error.
20 – 2F	Memory/Chipset: 2F is no memory detected or no useful memory detected.
30 – 3F	Recovery: 3F indicated recovery failure.
40 – 4F	Reserved for future use.
50 – 5F	I/O Busses: PCI, USB, ISA, ATA, etc. 5F is an unrecoverable error. Start with PCI.
60 – 6F	Reserved for future use (for new busses).
70 – 7F	Output Devices: All output consoles. 7F is an unrecoverable error.
80 – 8F	Reserved for future use (new output console codes).
90 – 9F	Input devices: Keyboard/Mouse. 9F is an unrecoverable error.
A0 – AF	Reserved for future use (new input console codes).
B0 – BF	Boot Devices: Includes fixed media and removable media. BF is an unrecoverable error.
C0 – CF	Reserved for future use.
D0 – DF	Boot device selection.
E0 – FF	F0 – FF: FF processor exception. E0 – EE: Miscellaneous codes. See Table 43. EF boot/S3: resume failure.

Table 43. Port 80h POST Codes

POST Code	Description of POST Operation
	Host Processor
10	Power-on initialization of the host processor (Boot Strap Processor)
11	Host processor Cache initialization (including APs)
12	Starting Application processor initialization
13	SMM initialization
	Chipset
21	Initializing a chipset component
	Memory
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
24	Programming timing parameters in the memory controller and the DIMMs
25	Configuring memory
26	Optimizing memory settings
27	Initializing memory, such as ECC init
28	Testing memory
	PCI Bus
50	Enumerating PCI busses
51	Allocating resources to PCI bus
52	Hot Plug PCI controller initialization
53 – 57	Reserved for PCI Bus
	USB
58	Resetting USB bus
59	Reserved for USB
	ATA/ATAPI/SATA
5A	Resetting PATA/SATA bus and all devices
5B	Reserved for ATA
	SMBus
5C	Resetting SMBUS
5D	Reserved for SMBUS
	Local Console
70	Resetting the VGA controller
71	Disabling the VGA controller
72	Enabling the VGA controller
	Remote Console
78	Resetting the console controller
79	Disabling the console controller
7A	Enabling the console controller

continued

Table 43. Port 80h POST Codes (continued)

POST Code	Description of POST Operation
	Keyboard (PS2 or USB)
90	Resetting keyboard
91	Disabling the keyboard
92	Detecting the presence of the keyboard
93	Enabling the keyboard
94	Clearing keyboard input buffer
95	Instructing keyboard controller to run Self Test (PS2 only)
	Mouse (PS2 or USB)
98	Resetting mouse
99	Detecting mouse
9A	Detecting presence of mouse
9B	Enabling mouse
	Fixed Media
B0	Resetting fixed media
B1	Disabling fixed media
B2	Detecting presence of a fixed media (IDE hard drive detection etc.)
B3	Enabling/configuring a fixed media
	Removable media
B8	Resetting removable media
B9	Disabling removable media
BA	Detecting presence of a removable media (IDE, CD-ROM detection, etc.)
BC	Enabling/configuring a removable media
	BDS
D*y*	Trying boot selection y (y=0 to 15)
	PEI Core
E0	Started dispatching PEIMs (emitted on first report of EFI_SW_PC_INIT_BEGIN EFI_SW_PEI_PC_HANDOFF_TO_NEXT
E2	Permanent memory found.
E1, E3	Reserved for PEI/PEIMs
	DXE Core
E4	Entered DXE phase
E5	Started dispatching drivers
E6	Started connecting drivers

continued

Table 43. Port 80h POST Codes (continued)

POST Code	Description of POST Operation
	DXE Drivers
E7	Waiting for user input
E8	Checking password
E9	Entering BIOS setup
EA	TBD – Flash Update
EB	Calling Legacy Option ROMs
EE	TBD – Calling INT 19. One beep unless silent boot is enabled.
EF	TBD – Unrecoverable Boot failure/S3 resume failure
	Runtime Phase/EFI OS Boot
F4	Entering Sleep state
F5	Exiting Sleep state
F8	EFI boot service ExitBootServices ( ) has been called
F9	EFI runtime service SetVirtualAddressMap ( ) has been called
FA	EFI runtime service ResetSystem ( ) has been called
	PEIMs/Recovery
30	Crisis Recovery has initiated per User request
31	Crisis Recovery has initiated by software (corrupt flash)
34	Loading recovery capsule
35	Handing off control to the recovery capsule
3F	Unable to recover

Table 44. Typical Port 80h POST Sequence

POST Code	Description
21	Initializing a chipset component
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
25	Configuring memory
28	Testing memory
34	Loading recovery capsule
E4	Entered DXE phase
12	Starting Application processor initialization
13	SMM initialization
50	Enumerating PCI busses
51	Allocating resourced to PCI bus
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test
EB	Calling Video BIOS
58	Resetting USB bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
01	INT 19
00	Ready to boot.